

Fig. 1

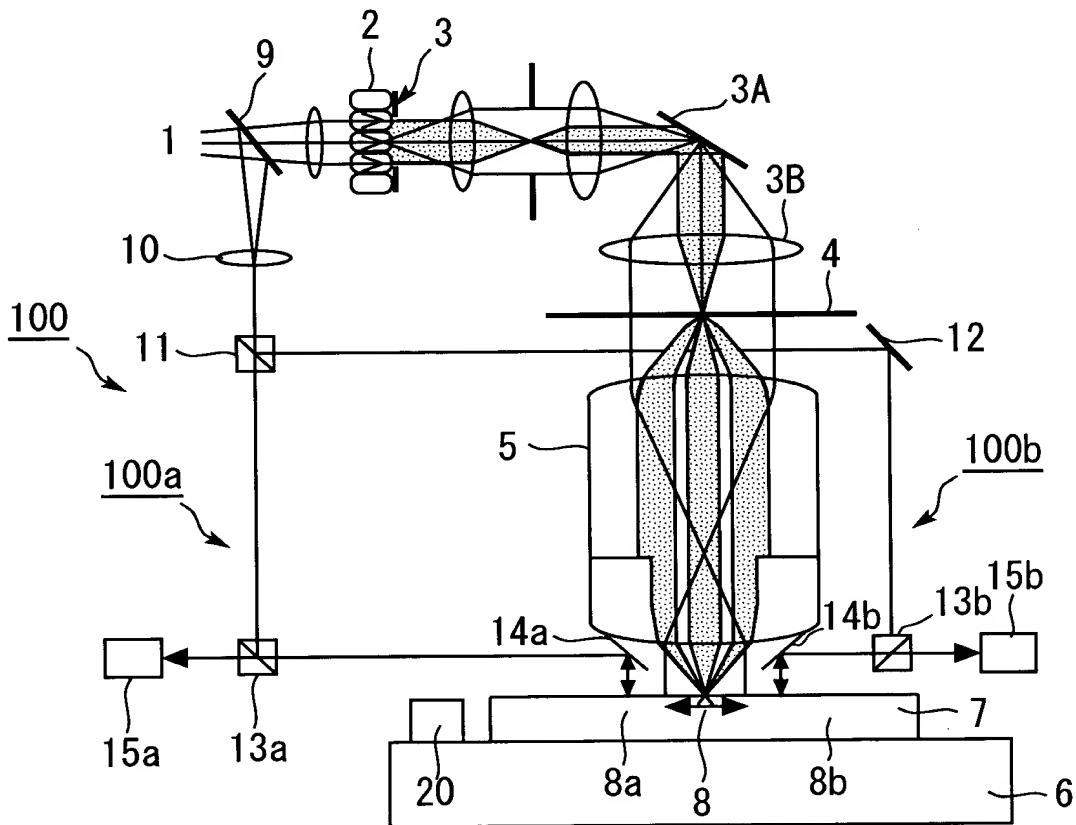
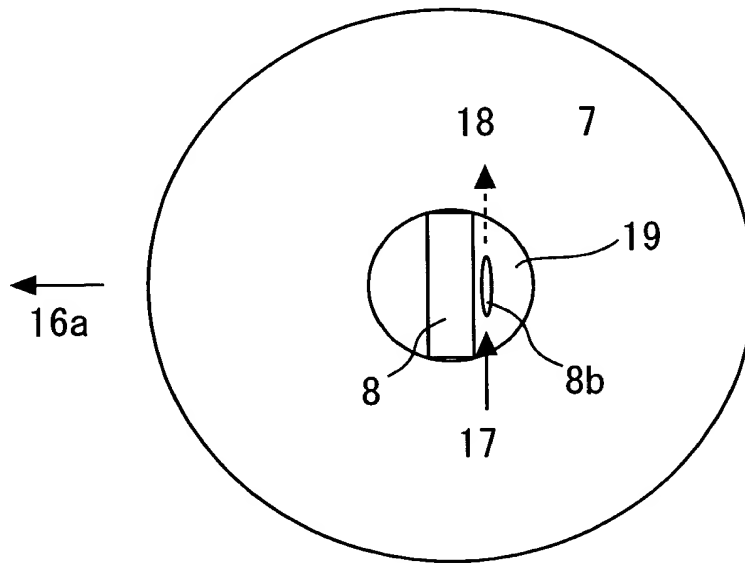


FIG. 1

*Fig. 2 A*



*Fig. 2 B*

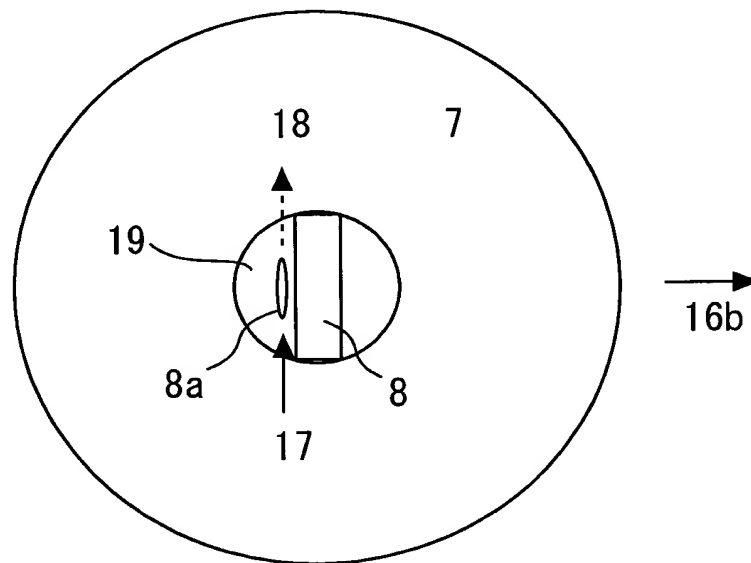


Fig. 3

PRIOR ART

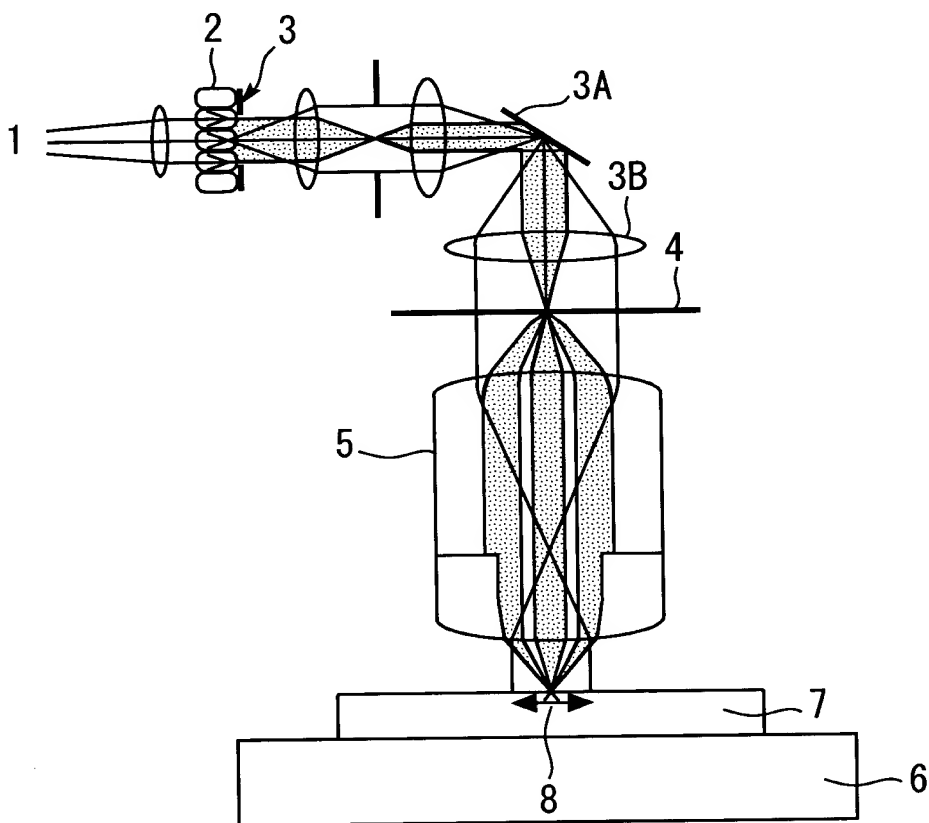


FIG. 3

Fig. 4

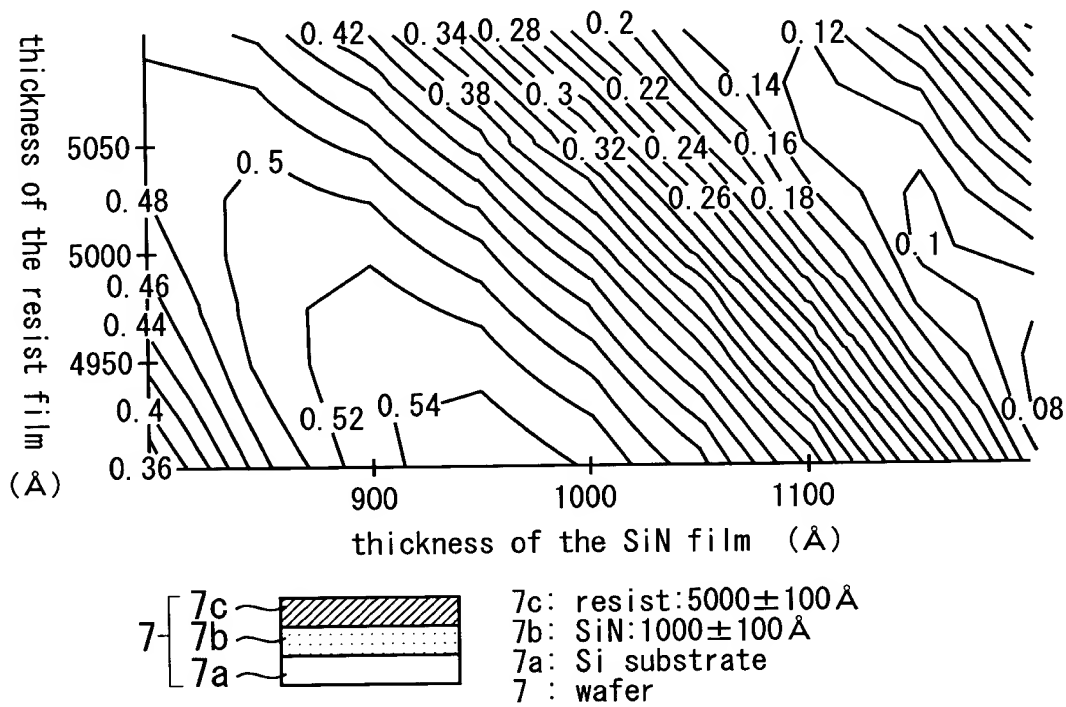
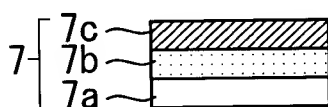
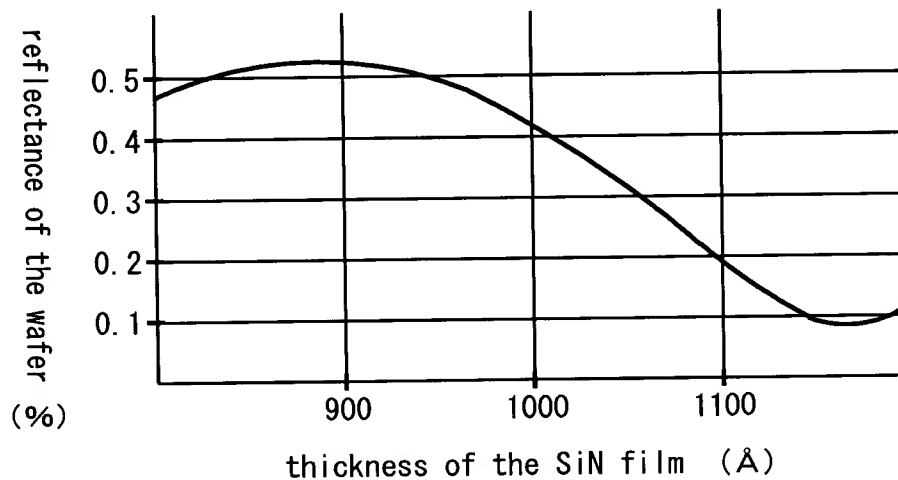
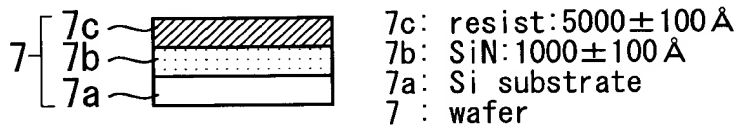
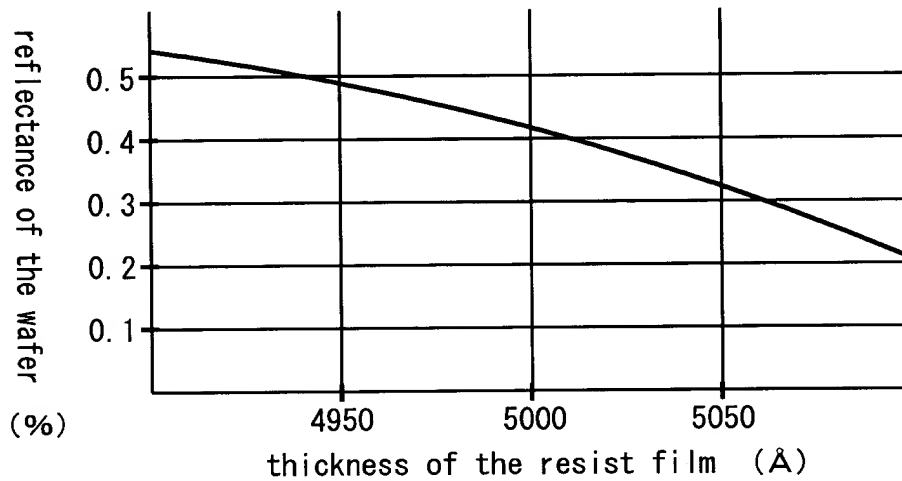


Fig. 5



7c: resist:  $5000 \pm 100 \text{ Å}$   
7b: SiN:  $1000 \pm 100 \text{ Å}$   
7a: Si substrate  
7: wafer

Fig. 6



[illegible]